PATENT
Customer No. 22,852
Attorney Docket No. 1165-763-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Shinya Kondoh	)	Group Art Unit: 2673
	)	
Serial No.: Not Yet Assigned	)	Examiner: A. Mengistu
	)	
Filed: Concurrently Herewith	)	
	)	
For: Antiferroelectric Liquid Crystal Display and Method of Driving the Same	)	

Commissioner for Patents and Trademarks
Washington, DC 20231

Sir:

PRELIMINARY AMENDMENT

Prior to the examination, please amend this application as follows:

IN THE ABSTRACT:

Cancel the Abstract and substitute the Abstract shown on the attached separate page.

IN THE SPECIFICATION:

Page 2, replace the paragraphs beginning on line 30 and ending on page 4, line 10 with the following new paragraph:

In accordance with an aspect of the present invention, an antiferroelectric liquid crystal panel, having an antiferroelectric liquid crystal between a pair of substrates, which comprises a driving circuit adapted to output a layer structure controlling voltage

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waveform having a frequency of 1 Hz to 100 Hz and a voltage in the range of +10 V to +50 V or -10 V to -50 V, for an optional length of time.

Page 4, replace the paragraph beginning on line 19 with the following new paragraph:

Figures 3a-3c are diagrams showing driving voltage waveforms for antiferroelectric liquid crystal according to the conventional art, and Figure 3d is their corresponding light transmittance.

Page 4, replace the paragraph beginning on line 23 with the following new paragraph:

Figures 4a-4c are diagrams showing the smectic layer structure within an antiferroelectric liquid crystal cell.

Page 4, replace the paragraph beginning on line 28 with the following new paragraph:

Figure 6 is a diagram showing an example of the variation of light transmittance with temperature history of the antiferroelectric liquid crystal when no voltage is applied.

Page 4, replace the paragraph beginning on line 33 with the following new paragraph:

Figures 8a-8c are diagrams showing a waveforms when the display driving voltage waveform for antiferroelectric liquid crystal shown in Figures 3a-3c are set so that the peak value of the scanning voltage applied during the non-selection period becomes equal to the peak value of the voltage applied during the selection period and Figure 8d is their corresponding light transmittance.

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Page 6, replace the paragraph beginning on line 31 with the following new paragraph:

Figures 3a-3c are diagrams showing display driving voltage waveforms for an antiferroelectric liquid crystal, and Figure 3d is their corresponding light transmittance, according to the conventional art. As shown in Figures 3a-3c, writing to a pixel is accomplished by applying a scanning voltage (3a) to a scanning electrode and a signal voltage (3b) to a signal electrode and thereby applying the resulting composite voltage 3c to the pixel which is formed from a liquid crystal element. According to the conventional art, when driving an antiferroelectric liquid crystal display, the first or second ferroelectric state or the antiferroelectric state is selected in a selection period (Se), and the selected state is held throughout the following non-selection period (NSe), as shown in Figures 3a-3c. That is, a selection pulse is applied in the selection period (Se), and the light transmittance (d) obtained as the result of the selection is maintained throughout the following non-selection period (NSe) to produce the display.

Page 7, replace the paragraph beginning on line 12 with the following new paragraph:

In an antiferroelectric liquid crystal display device, it is generally practiced to reset the antiferroelectric liquid crystal to the first or second ferroelectric state or the antiferroelectric state immediately before writing to the pixel. For example, in Figures 3a-3c, each selection period (Se) is immediately preceded by a reset period (Rs). During this reset period, a voltage lower than the threshold voltage is applied to the pixel to reset the antiferroelectric liquid crystal to the antiferroelectric state. By resetting the state of each pixel in this way immediately before writing necessary

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information to the pixel, a good display can be produced with each pixel being unaffected by its previously written state.

Page 7, replace the paragraph beginning on line 26 with the following new paragraph:

In Figures 3a-3d, F1, F2, F3, and F4 denote the first, second, third, and fourth frames, respectively. In this waveform diagram, a white display is produced in the first and second frames, and a black display is produced in the third and fourth frames. The voltage polarity is usually reversed from one frame to the next, as shown in the figure.

Page 8, replace the paragraph beginning on line 2 with the following new paragraph:

Figures 4a-4c are diagrams showing the layer structure formed within the ferroelectric liquid crystal cell; as shown, a liquid crystal layer 20 is sandwiched between a pair of glass substrates 21a and 21b. Immediately after the liquid crystal is injected into the liquid crystal panel, the layer structure is the chevron structure with the layers bent in the middle between the top and bottom glass substrates, as shown in Figure 4a. When the layer structure controlling voltage waveform is applied, the layer structure changes to the bookshelf structure with the layers lying perpendicular to the top and bottom substrates, as shown in Figure 4b. If the temperature changes thereafter, causing a change in the smectic layer spacing, the layer structure changes to a structure similar to the initial chevron structure, as shown in Figure 4c. Thereafter, when the display voltage waveform is applied to the liquid crystal cell, the layer structure changes to a quasi-bookshelf structure in the case of a white display, while in the case

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of a black display, the layer structure remains substantially unchanged and the layer structure shown in Figure 4c is retained.

Page 9, replace the paragraph beginning on line 3 with the following new paragraph:

Figure 6 shows an example of the variation of light transmittance with temperature history when no voltage is applied. In the liquid crystal panel comprising a liquid crystal device having the property that the layer spacing dR is the smallest at room temperature TR, the temperature of the liquid crystal panel was lowered from TR to TL, then raised back to TR. Figure 6 shows the relationship between the light transmittance and the temperature during the process of this temperature history; as shown, the light transmittance changed from point A to point B, then to point C. That is, in this example, when the temperature was lowered from TR to TL, the light transmittance decreased from a% to b%, but when the temperature was raised from TL to TR, the light transmittance increased and reached c% at point C. On the other hand, when the temperature of the liquid crystal panel was raised from TR to TH and then lowered back to TR, the light transmittance changed from point A to pont D, then to point E. That is, in this example, when the temperature was raised from TR to TH, the light transmittance decreased from a% to b%, but when the temperature was lowered from TH to TR, the light transmittance increased and reached e% at point E.

Page 10, replace the paragraph beginning on line 29 with the following new paragraph:

Figures 8a-8c show waveforms when the display driving voltage waveform for antiferroelectric liquid crystal shown in Figures 3a-3c are set so that the peak value of

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the scanning voltage applied during the non-selection period (NSe) becomes equal to the peak value of the voltage applied during the selection period (Se). In Figures 8a-8d, (8a) is the scanning voltage waveform, (8b) is the signal voltage waveform, (8c) is the composite voltage waveform, and 8d is the light transmittance. The waveform shown in Figure 8a provides a voltage waveform close to the layer structure controlling voltage waveform.

Page 11, replace the paragraph beginning on line 5 with the following new paragraph:

The waveforms shown in Figures 8a-8c have a reset period (Rs) and the layer structure controlling voltage waveform is not applied in this period. However, if the peak value of the scanning voltage waveform is made the same for all periods (selection period, non-selection period, and reset period) within one frame, a more effective layer structure controlling voltage waveform can be produced. In view of this, the length of the reset period is made adjustable in the voltage waveform shown in Figures 8a-8c. Figure 9 shows the waveform when the reset period (Rs) is set to 0. The driving voltage waveform control circuit 11 shown in Figure 10 controls the scanning voltage waveform generating circuit 13 to control the reset period.

Page 13, replace the paragraph beginning on line 9 with the following new paragraph:

In the present invention, normally the driving waveform shown in Figures 3a-3c are applied to the liquid crystal to produce the display. On the other hand, when, for example, the temperature of the liquid crystal panel 10 drops from room temperature to a temperature lower than 10°C and then rises above 10°C, the layer structure changes

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and the "image sticking phenomenon" occurs. In such a case, the layer structure controlling voltage waveform shown in Figure 8 is applied to the liquid crystal panel to alleviate the "image sticking phenomenon."

Page 13, replace the paragraph beginning on line 20 with the following new paragraph:

Figure 12 shows the scanning voltage waveform for the case when a temperature change occurs during application of the normal driving waveform and the contacts of the switches SW1 and SW2 of Figure 11 are switched from b to a to alleviate the "image sticking phenomenon" occurring due to the temperature change. As shown, the normal driving voltage waveform (in frames F1 to F4) is followed by the scanning voltage waveform (from frame F5 onward) of Figure 8(a) which is applied as the layer structure controlling voltage waveform to the liquid crystal. Using a scanning voltage waveform whose one frame period (the sum of the reset period, selection period, and non-selection period) is about 17 ms, a layer structure controlling voltage waveform, in which the peak value of the scanning voltage waveform applied during the selection period and the peak value of the scanning voltage waveform applied during the non-selection period were both set to ±30 V, was applied to the liquid crystal for about one second. As a result, the change in the geometry of the smectic layer structure due to the temperature change was corrected, and the "image sticking phenomenon" did not occur. Further, the application of the layer structure controlling voltage waveform had little effect on the display quality, since the application time was very short. The length of time over which the layer structure controlling voltage

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waveform is applied is determined by issuing an instruction from the driving voltage waveform control circuit 11 to the power supply circuit 15 in Figure 11.

Page 15, line 16, add the following paragraphs:

Summarizing the advantageous effects of the invention, explained above, the invention provides an antiferroelectric liquid crystal panel, having an antiferroelectric liquid crystal between a pair of substrates, which comprises a driving circuit adapted to output a layer structure controlling voltage waveform having a frequency of 1 Hz to 100 Hz and a voltage in the range of +10 V to +50 V or -10 V to -50 V, for an optional length of time.

In the above antiferroelectric liquid crystal panel, the optional length of time is equal to the overall period of one frame.

In the above antiferroelectric liquid crystal panel, the optional length of time is equal to the period of one frame excluding a reset period.

In the above antiferroelectric liquid crystal panel, the pair of substrates are provided with scanning electrodes and signal electrodes, and wherein the panel comprises a control circuit which outputs the layer structure controlling voltage waveform to the scanning electrodes.

The above antiferroelectric liquid crystal panel, comprising a temperature sensor and a control circuit which outputs the layer structure controlling voltage waveform in accordance with information from the temperature sensor.

The above antiferroelectric liquid crystal panel, comprising a control circuit which outputs the layer structure controlling voltage waveform, when the information from the

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temperature sensor indicates a temperature change that reduces the layer spacing in the antiferroelectric liquid crystal.

The above antiferroelectric liquid crystal panel, comprising a control circuit which outputs the layer structure controlling voltage waveform, for said optional length of time, at predetermined intervals of time.

The invention provides a method of driving an antiferroelectric liquid crystal panel having an antiferroelectric liquid crystal between a pair of substrates wherein a layer structure controlling voltage waveform having a frequency of 1 Hz to 100 Hz and a voltage in the range of +10 V to +50 V or -10 V to -50 V, is output for an optional length of time.

In the above method of driving an antiferroelectric liquid crystal panel, the optional length of time is equal to the overall period of one frame.

In the above method of driving an antiferroelectric liquid crystal panel, the optional length of time is equal to the period of one frame excluding a reset period.

In the above method of driving an antiferroelectric liquid crystal panel, the pair of substrates are provided with scanning electrodes and signal electrodes, and the layer structure controlling voltage waveform is output to the scanning electrodes.

In the above method of driving an antiferroelectric liquid crystal panel, the antiferroelectric liquid crystal panel comprises a temperature sensor and the layer structure controlling voltage waveform is output in accordance with information from the temperature sensor.

In the above method of driving an antiferroelectric liquid crystal panel, the layer structure controlling voltage waveform is output, when information from the temperature

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sensor indicates a temperature change that reduces the layer spacing in the antiferroelectric liquid crystal.

In the above method of driving an antiferroelectric liquid crystal panel, the layer structure controlling voltage waveform is output, for said optional length of time, at predetermined intervals of time.

IN THE CLAIMS:

Cancel claims 1-10 and substitute therefore the following new claims:

11. An antiferroelectric liquid crystal panel, having an antiferroelectric liquid crystal between a pair of substrates, which comprises a driving circuit adapted to output a layer structure controlling voltage waveform having a frequency of 1 Hz to 100 Hz and a voltage in the range of +10 V to +50 V or -10 V to -50 V, for an optional length of time.

12. An antiferroelectric liquid crystal panel, as claimed in claim 11, wherein said optional length of time is equal to the overall period of one frame.

13. An antiferroelectric liquid crystal panel, as claimed in claim 11, wherein said optional length of time is equal to the period of one frame excluding a reset period.

14. An antiferroelectric liquid crystal panel, as claimed in claim 11, wherein the pair of substrates are provided with scanning electrodes and signal electrodes, and wherein the panel comprises a control circuit which outputs the layer structure controlling voltage waveform to the scanning electrodes.

15. An antiferroelectric liquid crystal panel, as claimed in claim 11, comprising a temperature sensor and a control circuit which outputs the layer structure controlling voltage waveform in accordance with information from the temperature sensor.

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16. An antiferroelectric liquid crystal panel, as claimed in claim 11, comprising a control circuit which outputs the layer structure controlling voltage waveform, when the information from the temperature sensor indicates a temperature change that reduces the layer spacing in the antiferroelectric liquid crystal.

17. An antiferroelectric liquid crystal panel, as claimed in claim 11, comprising a control circuit which outputs the layer structure controlling voltage waveform, for said optional length of time, at predetermined intervals of time.

18. A method of driving an antiferroelectric liquid crystal panel having an antiferroelectric liquid crystal between a pair of substrates wherein a layer structure controlling voltage waveform having a frequency 1 Hz to 100 Hz and a voltage in the range of +10 V to +50 V or -10 V to -50 V, is output for an optional length of time.

19. A method of driving an antiferroelectric liquid crystal panel, as claimed in claim 18, wherein said optional length of time is equal to the overall period of one frame.

20. A method of driving an antiferroelectric liquid crystal panel, as claimed in claim 18, wherein said optional length of time is equal to the period of one frame excluding a reset period.

21. A method of driving an antiferroelectric liquid crystal panel, as claimed in claim 18, wherein the pair of substrates are provided with scanning electrodes and signal electrodes, and wherein the layer structure controlling voltage waveform is output to the scanning electrodes

22. A method for driving an antiferroelectric liquid crystal panel as claimed in claim 18, wherein the antiferroelectric liquid crystal panel comprises a temperature

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sensor and the layer structure controlling voltage waveform is output in accordance with information from the temperature sensor.

23. A method of driving an antiferroelectric liquid crystal panel, as claimed in claim 18, wherein the layer structure controlling voltage wave form is output, when information from the temperature sensor indicates a temperature change that reduces the layer spacing in the antiferroelectric liquid crystal.

24. A method of driving an antiferroelectric liquid crystal panel, as claimed in claim 18, wherein the layer structure controlling voltage waveform is output, for said optional length of time, at predetermined intervals of time.

REMARKS

Examination of claims 11-24 in this continuation application is requested.

The specification has been amended to reflect the scope of the new claims and for clarity. It is believed the claims are supported by the application as filed and the claims and amendments to the specification do not add any new matter.

In addition, enclosed are proposed drawing corrections to Figs. 3, 4, and 8. Formal correction will be deferred pending allowability of the claims.

If there is any fee due in connection with the filing of this Preliminary Amendment, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: October 19, 2001

By: _____
Arthur S. Garrett
Reg. No. 20,338

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ABSTRACT

An antiferroelectric liquid crystal panel, having an antiferroelectric liquid crystal between a pair of substrates, which comprises a driving circuit adapted to output a layer structure controlling voltage waveform having a frequency of 1 Hz to 100 Hz and a voltage in the range of +10 V to +50 V or -10 V to -50 V, for an optional length of time.

Fig.3

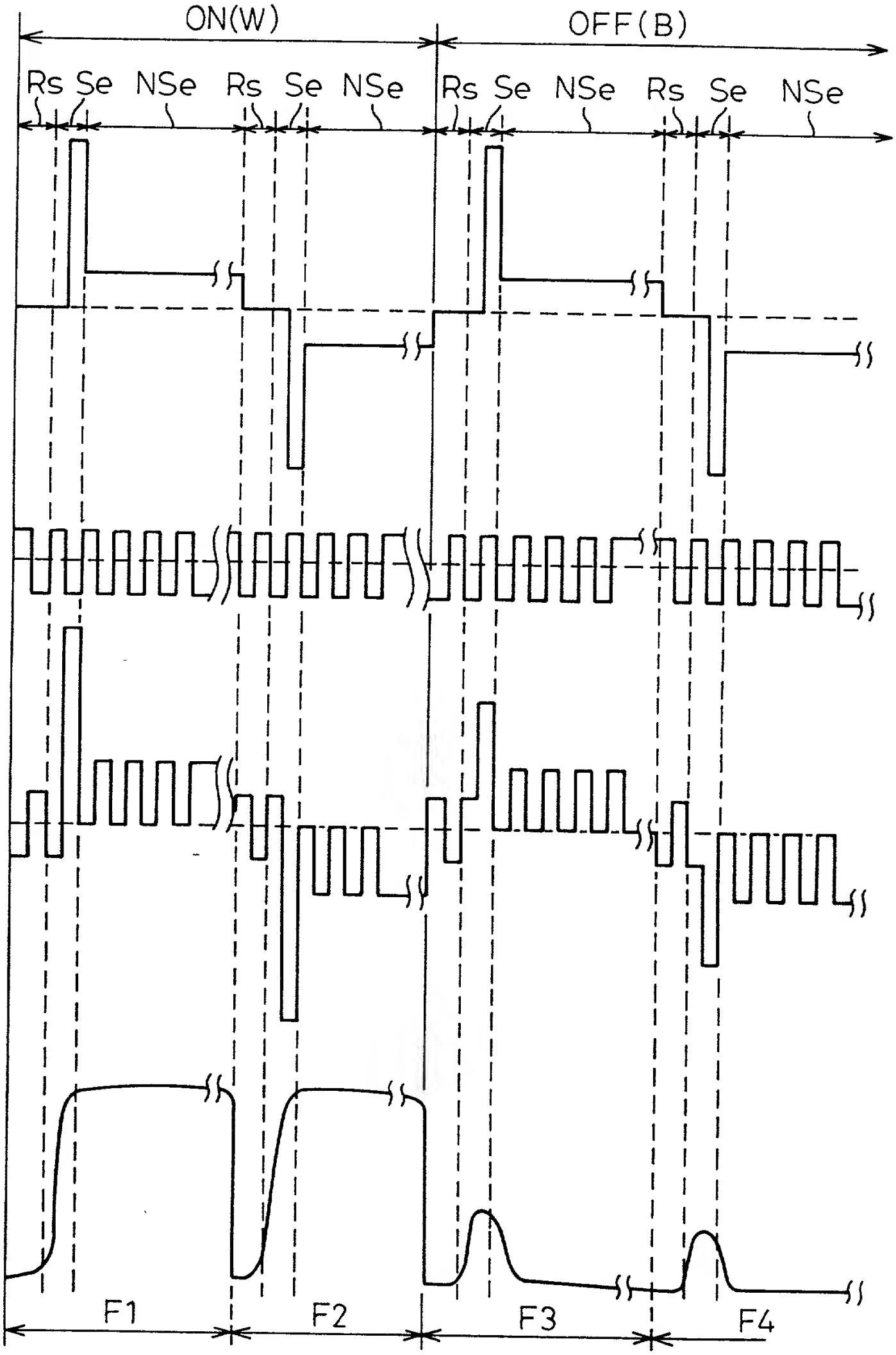

Fig. 3a (a)

Fig. 3b (b)

Fig. 3c (c)

Fig. 3d (d)

Fig.4

Fig4a

(a)

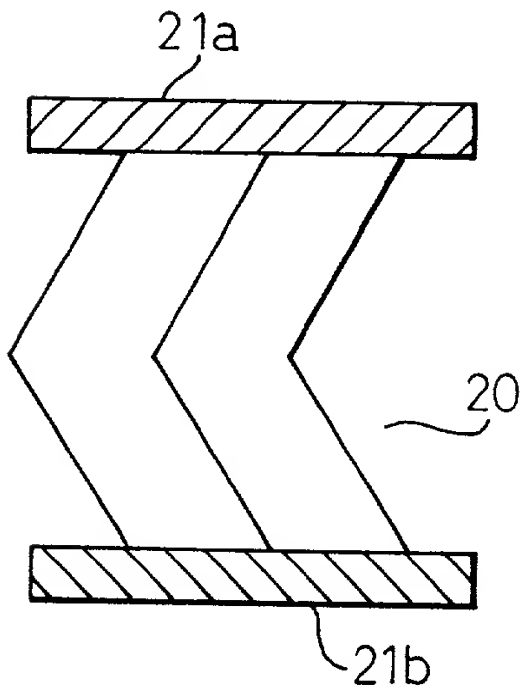

Fig4b

(b)

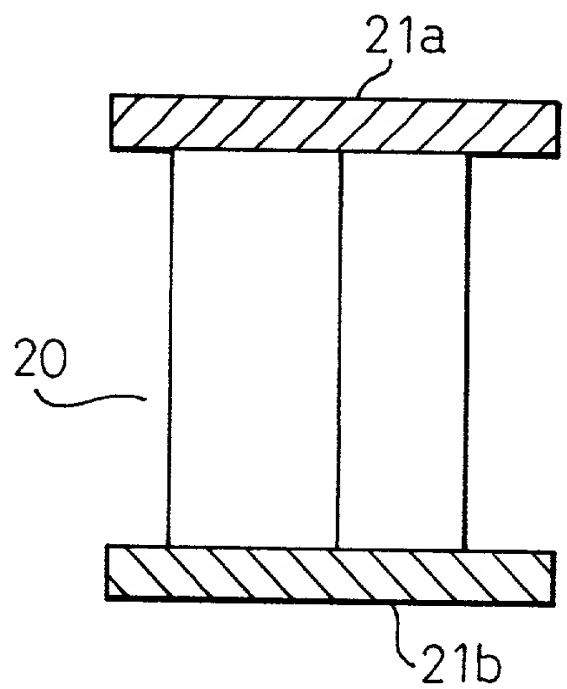

Fig4c

(c)

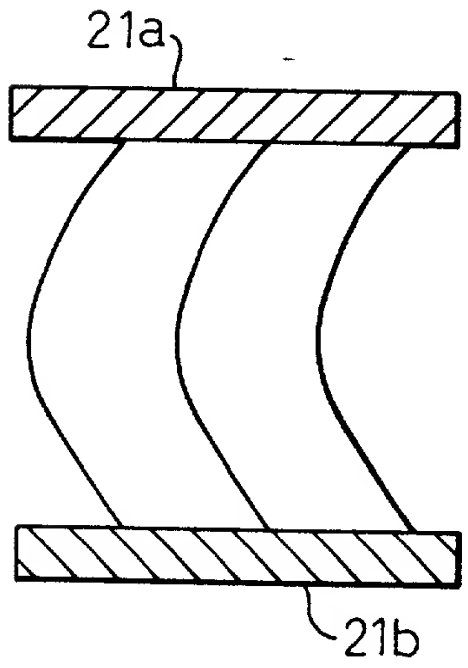

Fig.8

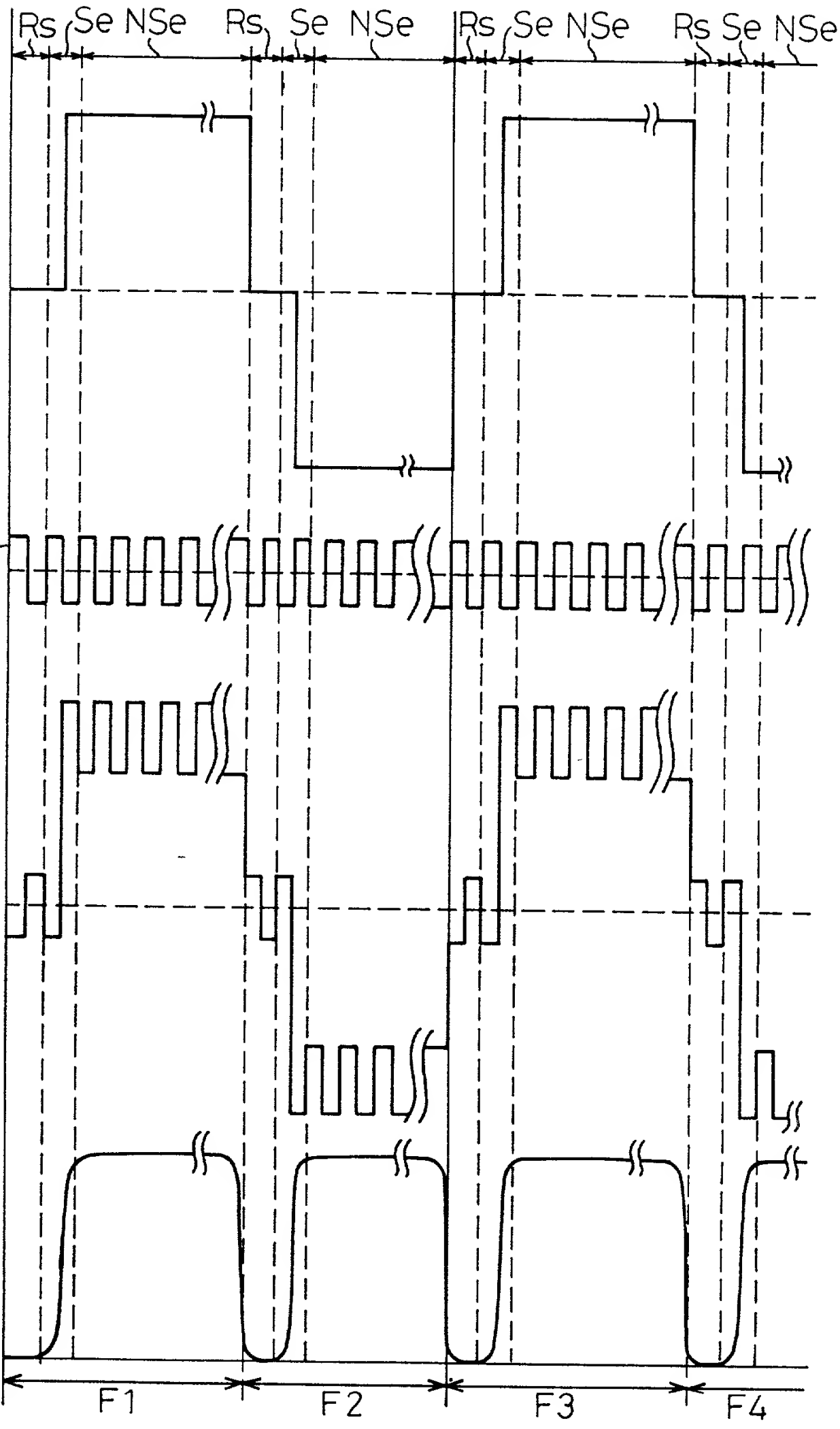

FIG 8a (a)

FIG 8b (b)

FIG 8c (c)

FIG 8d (d)

Application Number: Not Yet Assigned
Filing Date: Concurrently Herwith
Attorney Docket Number: 1165-763-1

APPENDIX TO PRELIMINARY AMENDMENT OF OCTOBER 19, 2001

Version with Markings to Show Changes Made

Amendments to the Specification

Page 2, replace the paragraphs beginning on line 30 and ending on page 4, line 10 with the following new paragraph:

In accordance with an aspect of the present invention, an antiferroelectric liquid crystal panel, having an antiferroelectric liquid crystal between a pair of substrates, which comprises a driving circuit adapted to output a layer structure controlling voltage waveform having a frequency of 1 Hz to 100 Hz and a voltage in the range of +10 V to +50 V or -10 V to -50 V, for an optional length of time.

Page 4, replace the paragraph beginning on line 19 with the following new paragraph:

[Figure 3 is a diagram] Figures 3a-3c are diagrams showing driving voltage waveforms for antiferroelectric liquid crystal according to the conventional art, and Figure 3d is their corresponding light transmittance.

Page 4, replace the paragraph beginning on line 23 with the following new paragraph:

[Figure 4 is a diagram] Figures 4a-4c are diagrams showing the smectic layer structure within an antiferroelectric liquid crystal cell.

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Page 4, replace the paragraph beginning on line 28 with the following new paragraph:

Figure 6 is a diagram showing an example of the variation of light transmittance with temperature history of the antiferroelectric liquid crystal when no voltage is applied.

Page 4, replace the paragraph beginning on line 33 with the following new paragraph:

[Figure 8 is a diagram] Figures 8a-8c are diagrams showing a [waveform] waveforms when the display driving voltage waveform for antiferroelectric liquid crystal shown in [Figure 3 is] Figures 3a-3c are set so that the peak value of the scanning voltage applied during the non-selection period becomes equal to the peak value of the voltage applied during the selection period and Figure 8d is their corresponding light transmittance.

Page 6, replace the paragraph beginning on line 31 with the following new paragraph:

[Figure 3 is a diagram] Figures 3a-3c are diagrams showing display driving voltage waveforms for an antiferroelectric liquid crystal, and Figure 3d is their corresponding light transmittance, according to the conventional art. As shown in [Figure 3] Figures 3a-3c, writing to a pixel is accomplished by applying a scanning voltage [(a)](3a) to a scanning electrode and a signal voltage [(b)](3b) to a signal electrode and thereby applying the resulting composite voltage [(c)]3c to the pixel which is formed from a liquid crystal element. According to the conventional art, when driving an antiferroelectric liquid crystal display, the first or second ferroelectric state or the antiferroelectric state is selected in a selection period (Se), and the selected state is

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held throughout the following non-selection period (NSe), as shown in [Figure 3] Figures 3a-3c. That is, a selection pulse is applied in the selection period (Se), and the light transmittance (d) obtained as the result of the selection is maintained throughout the following non-selection period (NSe) to produce the display.

Page 7, replace the paragraph beginning on line 12 with the following new paragraph:

In an antiferroelectric liquid crystal display device, it is generally practiced to reset the antiferroelectric liquid crystal to the first or second ferroelectric state or the antiferroelectric state immediately before writing to the pixel. For example, in [Figure 3] Figures 3a-3c, each selection period (Se) is immediately preceded by a reset period (Rs). During this reset period, a voltage lower than the threshold voltage is applied to the pixel to reset the antiferroelectric liquid crystal to the antiferroelectric state. By resetting the state of each pixel in this way immediately before writing necessary information to the pixel, a good display can be produced with each pixel being unaffected by its previously written state.

Page 7, replace the paragraph beginning on line 26 with the following new paragraph:

In [Figure 3] Figures 3a-3d, F1, F2, F3, and F4 denote the first, second, third, and fourth frames, respectively. In this waveform diagram, a white display is produced in the first and second frames, and a black display is produced in the third and fourth frames. The voltage polarity is usually reversed from one frame to the next, as shown in the figure.

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Page 8, replace the paragraph beginning on line 2 with the following new paragraph:

[Figure 4 is a diagram] Figures 4a-4c are diagrams showing the layer structure formed within the ferroelectric liquid crystal cell; as shown, a liquid crystal layer 20 is sandwiched between a pair of glass substrates 21a and 21b. Immediately after the liquid crystal is injected into the liquid crystal panel, the layer structure is the chevron structure with the layers bent in the middle between the top and bottom glass substrates, as shown in Figure 4a [part (a) of the figure]. When the layer structure controlling voltage waveform is applied, the layer structure changes to the bookshelf structure with the layers lying perpendicular to the top and bottom substrates, as shown in [part (b) of the figure] Figure 4b. If the temperature changes thereafter, causing a change in the smectic layer spacing, the layer structure changes to a structure similar to the initial chevron structure, as shown in [part (c) of the figure] Figure 4c. Thereafter, when the display voltage waveform is applied to the liquid crystal cell, the layer structure changes to a quasi-bookshelf structure in the case of a white display, while in the case of a black display, the layer structure remains substantially unchanged and the layer structure shown in [part (c)] Figure 4c is retained.

Page 9, replace the paragraph beginning on line 3 with the following new paragraph:

Figure 6 shows an example of the variation of light transmittance with temperature history when no voltage is applied. In the liquid crystal panel comprising a liquid crystal device having the property that the layer spacing dR is the smallest at room temperature TR, the temperature of the liquid crystal panel was lowered from TR

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to TL, then raised back to TR. Figure 6 shows the relationship between the light transmittance and the temperature during the process of this temperature history; as shown, the light transmittance changed from point A to point B, then to point C. That is, in this example, when the temperature was lowered from TR to TL, the light transmittance decreased from a% to b%, but when the temperature was raised from TL to TR, the light transmittance increased and reached c% at point C. On the other hand, when the temperature of the liquid crystal panel was raised from TR to TH and then lowered back to TR, the light transmittance changed from point A to pont D, then to point E. That is, in this example, when the temperature was raised from TR to TH, the light transmittance decreased from a% to b%, but when the temperature was lowered from TH to TR, the light transmittance increased and reached e% at point E.

Page 10, replace the paragraph beginning on line 29 with the following new paragraph:

[Figure 8 shows] Figures 8a-8c show waveforms when the display driving voltage waveform for antiferroelectric liquid crystal shown in [Figure 3 is] Figures 3a-3c are set so that the peak value of the scanning voltage applied during the non-selection period (NSe) becomes equal to the peak value of the voltage applied during the selection period (Se). In [Figure 8, (a)] Figures 8a-8d, (8a) is the scanning voltage waveform, [(b)](8b) is the signal voltage waveform, [(c])(8c) is the composite voltage waveform, and [(d)] 8d is the light transmittance. The waveform [(a)] shown in Figure [8]8a provides a voltage waveform close to the layer structure controlling voltage waveform.

Page 11, replace the paragraph beginning on line 5 with the following new paragraph:

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The [waveform] waveforms shown in [Figure 8 has] Figures 8a-8c have a reset period (Rs) and the layer structure controlling voltage waveform is not applied in this period. However, if the peak value of the scanning voltage waveform is made the same for all periods (selection period, non-selection period, and reset period) within one frame, a more effective layer structure controlling voltage waveform can be produced. In view of this, the length of the reset period is made adjustable in the voltage waveform shown in [Figure 8] Figures 8a-8c. Figure 9 shows the waveform when the reset period (Rs) is set to 0. The driving voltage waveform control circuit 11 shown in Figure 10 controls the scanning voltage waveform generating circuit 13 to control the reset period.

Page 13, replace the paragraph beginning on line 9 with the following new paragraph:

In the present invention, normally the driving waveform shown in [Figure 3 is] Figures 3a-3c are applied to the liquid crystal to produce the display. On the other hand, when, for example, the temperature of the liquid crystal panel 10 drops from room temperature to a temperature lower than 10°C and then rises above 10°C, the layer structure changes and the "image sticking phenomenon" occurs. In such a case, the layer structure controlling voltage waveform shown in Figure 8 is applied to the liquid crystal panel to alleviate the "image sticking phenomenon."

Page 13, replace the paragraph beginning on line 20 with the following new paragraph:

Figure 12 shows the scanning voltage waveform for the case when a temperature change occurs during application of the normal driving waveform and the contacts of the switches SW1 and SW2 of Figure 11 are switched from b to a to

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alleviate the "image sticking phenomenon" occurring due to the temperature change. As shown, the normal driving voltage waveform (in frames F1 to F4) is followed by the scanning voltage waveform (from frame F5 onward) of Figure 8(a) which is applied as the layer structure controlling voltage waveform to the liquid crystal. Using a scanning voltage waveform whose one frame period (the sum of the reset period, selection period, and non-selection period) is about 17 ms, a layer structure controlling voltage waveform, in which the peak value of the scanning voltage waveform applied during the selection period and the peak value of the scanning voltage waveform applied during the non-selection period were both set to ±30 V, was applied to the liquid crystal for about one second. As a result, the change in the geometry of the smectic layer structure due to the temperature change was corrected, and the "image sticking phenomenon" did not occur. Further, the application of the layer structure controlling voltage waveform had little effect on the display quality, since the application time was very short. The length of time over which the layer structure controlling voltage waveform is applied is determined by issuing an instruction from the driving voltage waveform control circuit 11 to the power supply circuit 15 in Figure 11.